REMARKS / ARGUMENTS

Claims 1-30 are pending in the application. Claims 1, 6, 16, and 25 have been amended. Claims 3-5 have been cancelled.

Claims 1 and 11-12 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S Patent No. 5,761,501 to Lubbers et al. (Hereinafter "Lubbers"). Claims 1-3, 7-14, 16-20, 25-27, and 29-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S Patent No. 6,272,033 to Watt (Hereinafter "Watt") in view of Lubbers. Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Watt in view of Lubbers in further view of U.S Patent No. 5,860,105 to McDermott (Hereinafter "McDermott"). Claims 15 and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Watt in view of Lubbers in further view of U.S Patent No. 5,724,550 to Stevens (Hereinafter "Stevens"). Claims 21-24 are allowed. Claims 5-6 are objected to as being dependent on a rejected base claim.

Rejections under 35 U.S.C. §102

Claims 1 and 11-12 are rejected under 35 U.S.C. §102(b) as being anticipated by Lubbers. Lubbers discloses a stacked skip list data structure for maintaining select nodes on multiple lists (*See* Abstract).

As stated in the Office Action, Lubbers does not contain one bit per a variable number of cache lines and wherein a logical arrangement of said list structure conforms to said variable number. Applicants respectfully submit, therefore, that elements of claim 1 are neither shown nor suggested by the cited reference. Claims 11-12 depend from claim 8 which depends from

claim 1. Accordingly, reconsideration and withdrawal of the rejection of claims 1 and 11-12 under 35 U.S.C. §102(b) is respectfully requested.

Claim Rejections under 35 U.S.C. §103(a)

Claims 1-3, 7-14, 16-20, 25-27, and 29-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Watt in view of Lubbers. Watt discloses a data processing apparatus having a memory storing a plurality of data words, a status bit store storing said status bits within a hierarchical relationship, and status querying logic determining a status of a data word within the memory (*See* Abstract).

As stated in the Office Action, neither Watt, Lubbers, nor any combination thereof contain one bit per a variable number of cache lines and wherein a logical arrangement of said list structure conforms to said variable number. Applicants respectfully submit, therefore, that elements of claim 1, 16, and 25 are neither shown nor suggested by the cited reference. Claims 2-3, 7-14, 17-20, 26-27, and 29-30 depend from claims 1, 16, and 25. Accordingly, reconsideration and withdrawal of the rejection of claims 1-3, 7-14, 16-20, 25-27, and 29-30 under 35 U.S.C. §103(a) is respectfully requested.

Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Watt in view of Lubbers in further view of McDermott. McDermott discloses an NDIRTY cache line lookahead technique used to expedite cache flush and export operations by providing a mechanism to avoid scanning at least some cache lines that do not contain dirty data (*See* Abstract).

As stated in the Office Action, neither Watt, Lubbers, McDermott nor any combination thereof contain one bit per a variable number of cache lines and wherein a logical arrangement of said list structure conforms to said variable number. Applicants respectfully submit, therefore, that elements of claim 1 are neither shown nor suggested by the cited reference. Claim 4 depends from claim 1. Accordingly, reconsideration and withdrawal of the rejection of claim 4 under 35 U.S.C. §103(a) is respectfully requested.

Claims 15 and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Watt in view of Lubbers in further view of Stevens. Stevens discloses circuit for responding to a microprocessor-generated write of a write-protected area of memory by invalidating a cache line corresponding to a write address in a microprocessor's internal cache by using a microprocessor address pin as a snoop invalidate signal during snoop cycles (*See* Abstract).

As stated in the Office Action, neither Watt, Lubbers, Stevens nor any combination thereof contain one bit per a variable number of cache lines and wherein a logical arrangement of said list structure conforms to said variable number. Applicants respectfully submit, therefore, that elements of claim 1 and 25 are neither shown nor suggested by the cited reference. Claims 15 and 28 depend from claims 1 and 25. Accordingly, reconsideration and withdrawal of the rejection of claims 15 and 28 under 35 U.S.C. §103(a) is respectfully requested.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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